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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,701	08/08/2002	Chun-Yi Yang	7744-US-PA	9328

31561 7590 03/22/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,701	YANG ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (6,440,803) or Shiau (6,372,580).

The claimed invention is directed to a method for fabricating a Mask ROM with self-aligned coding. A plurality of buried bit lines are formed in a substrate, and then a plurality of word lines are formed on the substrate crossing over the buried bit lines with first blocking strips thereon. A plurality of second blocking strips are formed between the word lines and between the first blocking strips, and then the first blocking strips are patterned into an array of blocking bumps, which define a plurality of pre-coding windows with the second blocking strips. A coding mask layer is formed on the substrate with a plurality of coding windows therein exposing selected pre-coding windows, and then a coding implantation is performed to form implanted coding regions in the substrate under the selected pre-coding regions exposed by the coding windows. The coding mask layer is then removed.

Accordingly, this invention provides a method for fabricating a Mask ROM with self-aligned coding without using a photo-mask with small aperture sizes, so as to reduce the fabrication cost of the photo-mask. Since the blocking bumps and the second blocking strips together define the pre-coding windows and block the regions outside the coding regions, the coding implantation can self-align to the coding regions under the coding windows to avoid

coding errors even if misalignment occurs. Therefore, the coding windows can be formed larger without causing coding errors.

Huang et al. teach a method of fabricating a mask ROM, comprising the steps of: forming a plurality of conductive strips on a substrate, wherein each conductive strip is formed with a cap layer on it; forming a first spacer and a second spacer on side-walls of each conductive strip, while the substrate under the first spacer is a first coding region and the substrate under the second spacer is a second coding region; forming a plurality of buried bit-lines in the substrate between the conductive strips, forming a first coding mask over the substrate, then performing a first tilt coding implantation to dope a part of the first coding regions; removing the first coding mask; forming a second coding mask over the substrate, then erforming a second tilt coding implantation to dope a part of the second coding regions; removing the second coding mask; removing the cap layer; forming a first conductive layer over the substrate; and patterning the first conductive layer and the conductive strips successively to form a plurality of word-lines and a plurality of gates, respectively.

And further comprising forming a raised bit-line on each buried bit-line after the second mask layer is removed and before the cap layer is removed.

Huang et al. also teaches a method of fabricating a mask ROM, in which larger coding windows can be formed to increase the margin of the coding process.

Shiau teaches a high density mask-type read only memory (ROM) device and a method of fabricating the high density mask-type read only memory (ROM) device using a salicide process. The method utilizes buried N+ bit lines, thick oxides for forming non-programmable cells, thin gate oxides in regions in which the thick field oxide has been removed to form programmable cells, polysilicon gate structures as word lines, and deposition of a single silicide

layer. Since only one silicide layer is deposited, the manufacturing process requires less steps. The resultant ROM device has a silicide layer over the word lines and portions of the buried bit lines that serves to reduce word line and bit line resistance. This results in a ROM device with improved operational speed of the memory cells.

After removal of the first photoresist layer, a second photoresist layer (31) is applied and patterned to expose areas of the substrate that will constitute the channel regions of the cells that can be set to an ON state when the word line voltage is high. Photolithography is then utilized to define coding openings (41) in this photoresist layer. This is illustrated in FIGS. 7A-D. Coding openings selectively expose the substrate surface, allowing subsequent formation of a thin gate oxide (33) on the exposed surface. The second photoresist layer is then removed.

Conventional techniques are then used to grow the gate oxide and its thickness depends on the process being used. Formation of the gate oxide is shown in FIGS. 8A-D. As shown in FIG. 8A, the thickness of the gate oxide layer is thicker over the BN+ regions. This is due to the faster oxidation rate of the doped silicon which results in higher dopant density and, thus, a thicker oxide.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Rosasco whose telephone number is 571-272-1389. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff, can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

For general Information call (571-272-1700).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
3/11/04